REMARKS

I. Summary of the Office Action

Claims 1-3 and 5-34 were pending in this application.

Claims 1-3, 5-24, 27-30, and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Patterson et al. U.S. Patent No. 6,653,957 (hereinafter "Patterson").

Claims 25, 26, 31, 33, and 34 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

II. Summary of Applicants' Reply

Applicants note with appreciation the indication of allowable subject matter in claims 25, 26, 31, 33, and 34 and hereby expressly reserve the right to rewrite any one of those claims in independent form should their base claims ultimately not be allowed.

Applicants have amended claims 1, 17, 18, and 22 to more particularly define the subject matter of the claimed invention. Applicants have also amended claim 27 to include the features of allowable claim 31 and have subsequently cancelled claim 31 without prejudice. These amendments are fully supported and justified by the application as originally filed. No new subject matter has been added.

The Examiner's claim rejection and objection are respectfully traversed.

III. The § 102(b) Rejection

Claims 1-3, 5-24, 27-30, and 32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Patterson. This rejection is respectfully traversed.

A. Independent Claim 1

Referring to FIG. 2 of Patterson, standard SERDES circuit 4 is modified to cooperate with a DC boundary scan test by including multiplexer 13, which selects normal mode traffic input 12 from 8B/10B encoder 11 during normal mode operation, or alternatively, boundary scan test data 15 during boundary scan test operation mode. The output of multiplexer 13 is sent to parallel-to-serial converter 25 and sent over serial link 5 to a serial-to-parallel converter which produces the received ten-bit parallel code. See Patterson, FIG.2, also column 6, lines 1-20.

The Examiner contends that encoder 11 of Patterson reads on applicants' claimed "first memory." (See Office Action, page 2, #2, line 2). This is simply not so. An encoder is at least functionally distinct from a memory. For example, encoder 11 in Patterson receives eight-bit parallel code data 3 and outputs an encoded 10-bit version 12 of that data. In contrast, memory circuits store and output data without substantial modification.

Furthermore, applicants are unable to find support in Patterson for the Examiner's contention that Patterson shows a circuit for synthesizing a clock signal of a particular frequency, as specified in applicant's independent claim 1. More specifically, applicants' claim 1 specifies, among other things, that the multiplexer circuitry is operative to select a predetermined sequence comprising at least one of each of first and second byte patterns. In contrast, multiplexer 13 of Patterson always

exclusively selects the output of 8B/10B encoder 11 during normal mode operation and does not intermix or selectively multiplex data between its two inputs to synthesize a clock signal. In addition, Patterson fails to show or suggest intermixing the contents of the signals from circuitries 17 and 19 to synthesize a clock signal. Therefore, Patterson fails to teach or suggest circuitry for synthesizing a clock signal as taught by applicants' claim 1.

Accordingly, for at least the foregoing reasons, applicants respectfully submit that independent claim 1 is allowable over Patterson. Dependent claims 2, 3, and 5-16 are also allowable for at least the reason they depend from allowable independent claim 1. Applicants therefore respectfully request that the rejection of these claims be withdrawn.

B. Independent Claim 17

Independent claim 17 specifies, among other things, transmission circuitry that synthesizes a clock signal having any one of a plurality of predetermined frequencies by serializing a predetermined sequence of first and second byte patterns. As discussed above under Section III-A, Patterson fails to show at least circuitry for synthesizing a clock signal by serializing a predetermined sequence of first and second byte patterns. Rather, the output of multiplexer 13 in Patterson consists exclusively of either input 12 from 8B/10B encoder 11 or boundary scan test data 15, not a sequence combining data from both inputs to synthesize a clock signal.

Accordingly, for at least the foregoing reason, applicants respectfully submit that independent claim 17 is allowable over Patterson. Dependent claims 18-22, and 24,

are also allowable for at least the reason they depend from allowable independent claim 17. Applicants therefore respectfully request that the rejection of these claims be withdrawn.

C. Independent Claim 27

Applicants have amended claim 27 to include all the features of now cancelled allowable claim 31. Accordingly, applicants respectfully submit that independent claim 27 is allowable for at least the reason previously pending claim 31 was allowable. Dependent claims 28-30, and 32 are also allowable for at least the reason they depend from allowable independent claim 27. Applicants therefore respectfully request that the rejection of these claims be withdrawn.

IV. The Objection to Claims 25, 26, 31, 33, and 34

Claims 25, 26, 31, 33, and 34 were objected to as being dependent upon a rejected base claim The Examiner's objection is respectfully traversed.

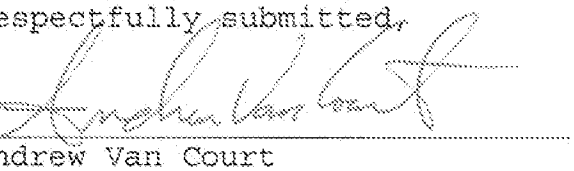
Claim 31 has been cancelled without prejudice, rendering its objection moot.

Claims 25, 26, 33, and 34 are allowable for at least the reason they depend from allowable independent claims 17 and 27. Applicants therefore respectfully request that the objection to these claims be withdrawn.

V. Conclusion

The foregoing has established that claims 1-3, 5-30, and 32-34 are in condition for allowance. Reconsideration and allowance of this application are accordingly respectfully requested.

Respectfully submitted,



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